Efficient FPGA Implementation of a STBC-OFDM Combiner for an IEEE 802.16 Software Radio Receiver

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Abstract

In this paper, an efficient FPGA implementation of a 4x4 Space-Time Block Coding (STBC) combiner for MIMO-OFDM software radio receivers is considered. The proposed combiner is based on a low-complexity algorithm which reduces the interference due to the Quasi-Orthogonality of the STBC decoding. In the literature, feedback techniques have been proposed to solve this problem. However, the algorithm introduced in this paper has been conceived in order to avoid the transmission feedback, by estimating the interference factors and removing them. The proposed algorithm exhibits a low computational complexity and complies with the requirements of HW feasibility, considering the execution time/area occupation trade-off.

1. Introduction

Multiple Input Multiple Output Orthogonal Frequency Division Multiplexing (MIMO-OFDM) techniques have been recently considered in the panorama of ongoing and future multimedia mobile communications due to their robustness to frequency-selective fading and their flexibility in handling multiple data rates. Nowadays, MIMO-OFDM techniques present some well-promising applications in wireless standards like IEEE 802.11n, E-UTRAN Long Term Evolution (LTE), and IEEE 802.16x (WiMax) [1]. Different Space-Time (ST) processing techniques have been proposed in the literature in order to fully exploit the potentialities of MIMO systems. The most popular one is Space-Time Coding [2], in which the time dimension is complemented with the spatial dimension inherent to the use of multiple spatially-distributed antennas. Commonly used ST coding schemes are ST-trellis codes and ST block codes (STBC). A well-known example of conceptually simple, computationally efficient and mathematically elegant STBC scheme has been proposed by Alamouti in [3]. Substantially, Alamouti's coding is an orthogonal ST block code where two successive symbols are encoded in an orthogonal 2x2 matrix. The columns of the matrix are transmitted in successive symbol periods, but the upper and the lower symbols in a given column are sent simultaneously through the first and the second transmit antennas, respectively.

The alternative solution to ST coding is represented by Spatial Multiplexing (SM) [4]. Spatial multiplexing is a space-time modulation technique whose core idea is to send independent data streams from each transmit antenna. This is motivated by the spatially white property of the distribution which achieves capacity in MIMO i.i.d. Rayleigh matrix channels. SM is addressed to push up link capacity rather than to exploit spatial diversity. The tradeoff is between spatial diversity exploitation (STBC) and capacity boosting (SM). Such tradeoff has been theoretically studied by Heath and Paulraj in [5] and some simulation results have been shown for a switch criterion from STBC to SM (and vice-versa) based on the minimum Euclidean distance of the received codebook. Recent contributions presented in literature are aimed at proposing practical

solutions for MIMO-OFDM ST processing to be specifically applied in the framework of on-going wireless standards. In their work [6], Bian et. al. considered a range of MIMO-OFDM architectures for use in urban hotspots in the framework of IEEE 802.11n. Link adaptation drives the choice of the space-time signal processing. In the urban areas tested in [6], 2% of the covered locations selected the SM scheme, 50% selected the STBC scheme, and 48% selected a hybrid SM/STBC scheme. The combination of SM and adaptive beamforming in MIMO-OFDM systems for IEEE 802.16e WMAN standard has been studied by Chung, Yung and Choi in [7]. In [8], Aruna and Suganthi proposed a variable power adaptive MIMO-OFDM STBC for WiMax in order to provide flexible data-rate services while satisfying low delay requirements in the presence of imperfect CSI knowledge.

In the present paper, a practical solution for the implementation of a Software-Defined-Radio (SDR) based Space-Time Block decoder for a 4x4 MIMO-OFDM receiver in the framework of IEEE 802.16x is proposed and tested. The SDR implementation of a STBC decoder is really challenging and presents some issues to be solved. The most relevant ones are related to the efficient implementation of the space-time diversity combiner. Such a block is very critical as in the 4x4 configuration it should be implemented by means of a pseudo-inversion of the channel matrix that is computationally expensive and may provide poor performance due to the noise increasing. Therefore, a computationally-affordable and interference-robust subtractive combiner is considered for the conceived receiver. In this work, the SDR-based implementation of the subtractive combiner is motivated and discussed, and results are shown in terms of Field Programmable Gate Array (FPGA) resource requirements and real-time execution capabilities.

The paper is structured as follows: in Section 2 some related works about SDR-based MIMO implementation are presented. Section 3 is devoted to describing the signal processing architecture of the proposed SDR-based STBC MIMO system. Section 4 focuses on the hardware implementation of the diversity combiner. Section 5 aims at presenting and discussing experimental results. Section 6 draws paper conclusions.

2. Related works

Our work is inserted in the state-of-the-art framework of SDR-based and FPGA-based MIMO receiver implementations. In fact, in this work, the problem of the implementation of a MIMO receiver has been addressed from a practical viewpoint, considering commercial HW platforms, characterized by a good tradeoff between efficiency and cost.

One of the first works dealing with SDR MIMO-OFDM prototyping has been proposed by Gupta, Forenza and Heat in [9]. The prototyping approach was targeted to the rapid deployment of a "ready-to-market" architecture based on flexible SDR and commercially available hardware. The software design of all main receiver functionalities added a great flexibility and ease of use to the designed architecture, at the price of throughput expense. Recent works like [10] and [11] are explicitly targeted at mapping the SDR architectural design of MIMO systems onto efficient commercial HW platforms able to support real-world wireless applications. In [10], the utilization of GNU Radio has been considered to program the physical and data-link layers of Universal Software Radio Peripheral (USRP) consisting of a motherboard for baseband processing, two daughter boards for RF frontend processing and an embedded Intel Core General Purpose Processing (GPP) unit hosting Linux OS. Using such a platform, a variety of multimedia delivery applications can be effectively supported on Mobile Ad-Hoc Networks (MANETs). In [11], a 40 MHz MIMO OFDM system with Space Division Multiplexing has been mapped onto a multi-processor SDR platform using two instances of state-of-the-art ADRES embedded processor. It has been shown in [11] that when the parallelization is wisely performed, it is possible to achieve the theoretical gain factor of two with respect to the single-processor system. Another interesting work has been proposed by Pan et al. in [12]; its authors considered the implementation of reconfigurable antennas in multi-radio platform.

By this preliminary state-of-the-art scanning, we can say that the emphasis of R&D in SDR-based MIMO systems is on the implementation of SW receiver architectures characterized by flexibility,

adaptivity and high degree of reprogrammability, with the clear objective of achieving high performances while keeping hardware costs reasonably low. In such a framework, the adoption of FPGA devices should represent a winner solution because of their reconfigurability and support of parallelism. FPGAs have been successfully employed in the implementation of complex receiver architectures working in broadband applications, like e.g., the RAKE receiver for Direct Sequence Ultra-Wideband (DS-UWB) communication systems presented in [13]. FPGAs can provide the modularity and parallelism required by such a computationally-demanding signal processing task. Coming back to the MIMO-OFDM implementation framework, Haene, Perles, and Burg proposed in [14] a FPGA-based 4-Stream MIMO-OFDM transceiver capable of transmitting 216 Mb/s in 20 MHz bandwidth. A linear detection algorithm is employed in [14] to combine spatial diversity. In the recent work of [15], Wang and Sobelman proposed a joint MIMO transceiver design based on uniform channel decomposition. This closed-loop MIMO system can run at 400 MHz with a 16-QAM constellation on a Xilinx Virtex-4 FPGA and can achieve a throughput of 12.8 Gb/s in a 8x8 MIMO configuration. Aspects of FPGA implementation of equalization and multi-user detection have been considered in MIMO and MIMO-OFDM systems in [16], [17] and [18]. In [16], Yu et. al. proposed an FPGA implementation of a maximum-likelihood decision-feedback equalization for MIMO system. An iterative receiver for MIMO-OFDM systems has been realized on an ALTERA STRATIX FPGA by Boher, Rabineau, and Hélard [17]. Finally, a sphere decoder for a 4x4 MIMO system has been implemented in [18] on a Xilinx XC2VP30 FPGA device with a MicroBlaze soft core processor. The hardware prototypes of [18] can support up to 81.5 Mb/s data rate at 20 dB signal-to-noise ratio, which is 97 times faster than their respective implementations in a digital signal processor.

The present work aims to provide a novel contribution to the state-of-the-art framework mentioned above by addressing the problem of the efficient FPGA implementation of the diversity combiner in a multi-antenna MIMO-OFDM scheme, considering in details basic issues like computational complexity, interference and noise reduction, real-time execution and efficient hardware resource

management. At our best knowledge such kind of aspects has been only partially considered in literature, without a specific attention to the issues related to the device implementation.

3. System Description and OFDM-STBC Signal Processing

The MIMO-OFDM system considered in this paper is based on the IEEE 802.16d standard [19], extended with the MIMO section. The IEEE 802.16 is the telecommunication standard on which the Worldwide Interoperability for Microwave Access (WiMAX) and the Wireless Metropolitan Area Network (WMAN) are based. These two are wireless technologies which provides high bit rate to the system. In particular, the paper is focused on the IEEE 802.16d-2004, based on OFDM transmission with TDMA as multiple access. In particular, the analysis carried out relies on different parts: the first one is related to software simulations and the second one to the hardware implementation and co-simulation. The simulation work deals with the test of MISO/MIMO encoding and decoding algorithms. The work done on the hardware focuses on the receiver side (decoder) and in particular considers the MIMO mode which has best simulation results between those treated (see Fig.1).

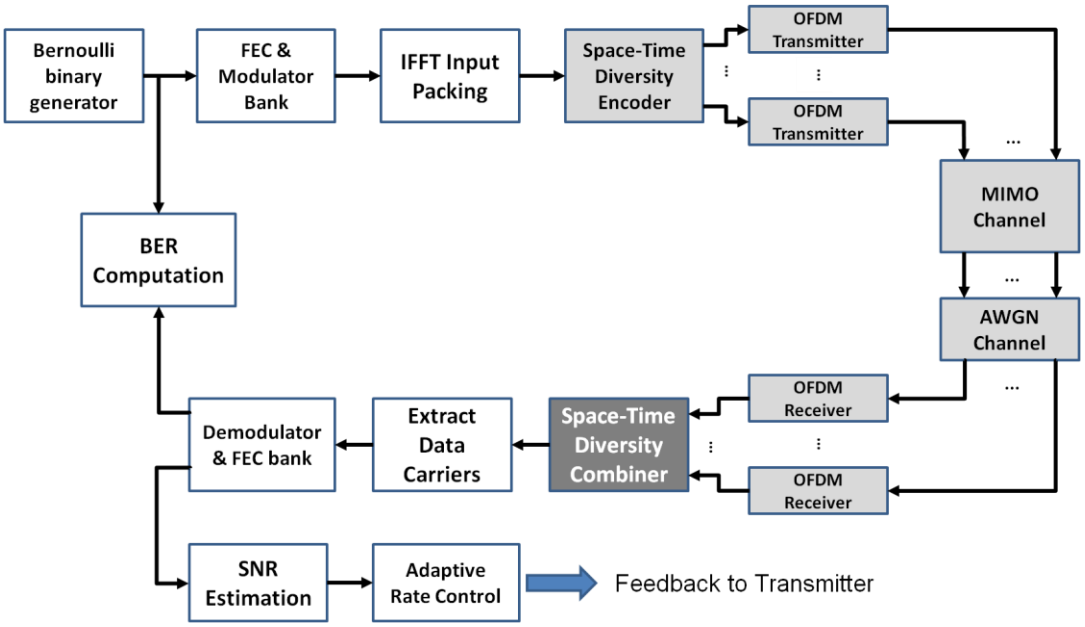


Figure 1. IEEE 802.16-2004 OFDM PHY-layer simulation scheme: the dark shaded blocks have been simulated and implemented on hardware; the light shaded blocks have been developed for the software simulations.

In the following of this section two different techniques, based on Alamouti's STBC, are considered, in the case of MISO 4x1 and MIMO 4x4. The investigated techniques are related to the receiver only, without considering any type of Channel State Information (CSI) feedback, nor pre-coding at the transmitter side. The only feedback available is the one related to the rate adaptation process. In particular, we refer to the "channel inversion" decoding technique and to the "subtractive combining" one. A detailed explanation of the two techniques is given in the next subsections. Furthermore, the performances of the four cases are evaluated through qualitative simulations and compared.

3.1 Multiple Input Single Output 4x1 case

The considered system consists of an extended 4 antennas STBC Alamouti transmitter and a combiner at the receiver that exploits the information of a single antenna only. Given the absence of feedback and the minimal number of antennas, it is not possible to expect from this case high performance, especially in terms of robustness to interference/errors.

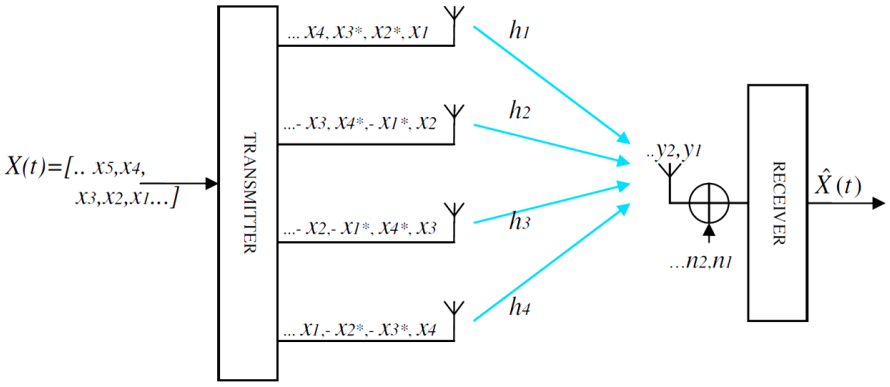


Figure 2. MISO 4x1 case: the transmitter at the left side exploits an extended Alamouti STBC transmission while a combiner at the receiver (right) side attempts to decode the transmitted streams.

The choice of a 4x MIMO instead of the usual 2x1 or 2x2 configurations is motivated by the necessity of increasing diversity in the space domain even though the system does not unleash all its potential with only one receiving antenna.

3.2 Channel Inversion Combiner

By extending the traditional STBC transmission scheme, the transmitted MISO symbol is hence given by:

$$X = \begin{bmatrix} x_1 & x_2 & x_3 & x_4 \\ x_2^* & -x_1^* & x_4^* & -x_3^* \\ x_3^* & x_4^* & -x_1^* & -x_2^* \\ x_4 & -x_3 & -x_2 & x_1 \end{bmatrix} \quad (1)$$

When attempting to decode the symbol with the traditional multiplication between the Hermitian channel matrix and the original H, as indicated in Equation (2), a square, non-diagonal matrix is obtained:

$$H^H \times H = \begin{bmatrix} \alpha & 0 & 0 & \beta \\ 0 & \alpha & -\beta & 0 \\ 0 & -\beta & \alpha & 0 \\ \beta & 0 & 0 & \alpha \end{bmatrix} \quad (2)$$

Assuming:

$$\alpha = |h_1|^2 + |h_2|^2 + |h_3|^2 + |h_4|^2 \quad (3)$$

and

$$\beta = 2 \cdot Re(h_1^* h_4 - h_3 h_2^*) \quad (4)$$

By normalizing the matrix with respect to α, it is possible to obtain a quasi-identity matrix:

$$\frac{1}{\alpha} H^H \times H = \begin{bmatrix} 1 & 0 & 0 & \beta/\alpha \\ 0 & 1 & -\beta/\alpha & 0 \\ 0 & -\beta/\alpha & 1 & 0 \\ \beta/\alpha & 0 & 0 & 1 \end{bmatrix} \quad (5)$$

The residual β/α affects the reception and the classical Alamouti's decoding, which is severely degraded without the usage of an explicit feedback to the transmitter.

It is then possible to "force" the receiver to derive a pure identity through the insertion of a decoding matrix:

$$H^H M H = I \tag{6}$$

After few simple passages it is possible to obtain that:

$$M = H^{H^{-1}} H^{-1} \tag{7}$$

So that the estimated received symbol becomes:

$$\tilde{X} = H^{-1} Y = X + H^{-1} N \tag{8}$$

which is the same modality used to decode a standard 2x2 SM, despite of the usage of a 4 antennas STBC system. While mathematically simple, this solution derived from an inverse problem is ill-posed, and then highly susceptible to the precision of the channel estimation.

3.3 Subtractive Combiner

In order to avoid the illness introduced by the pure inversion of the channel matrix, it is possible to exploit the direct estimation of the channel matrix in order to reduce the effect of the residuals. Even if this method is not free from error sources, these errors are linearly and directly dependent with the channel estimation instead of inversely.

If we try to decode the signal in the traditional STBC way, we obtain an estimated symbol:

$$\begin{bmatrix} \tilde{x}_1 \\ \tilde{x}_2 \\ \tilde{x}_3 \\ \tilde{x}_4 \end{bmatrix} = \begin{bmatrix} x_1 + \beta/\alpha \cdot x_4 \\ x_2 - \beta/\alpha \cdot x_3 \\ x_3 - \beta/\alpha \cdot x_2 \\ x_4 + \beta/\alpha \cdot x_1 \end{bmatrix} + \frac{1}{\alpha} H^H \times \begin{bmatrix} n_1 \\ n_2^* \\ n_3^* \\ n_4 \end{bmatrix} \tag{9}$$

where it is clear the effect of the residuals in the decoding process.

Let us now introduce a new vector:

$$\begin{bmatrix} \hat{x}_1 + \beta/\alpha \cdot \hat{x}_4 \\ \hat{x}_2 - \beta/\alpha \cdot \hat{x}_3 \\ \hat{x}_3 - \beta/\alpha \cdot \hat{x}_2 \\ \hat{x}_4 + \beta/\alpha \cdot \hat{x}_1 \end{bmatrix} = \frac{1}{\alpha} \begin{bmatrix} A \\ B \\ C \\ D \end{bmatrix} \tag{10}$$

where the $\hat{x}_i$ are decoded values under the assumption that the contribution of the noise N is negligible. In this way it is possible to derive the estimated vector as:

$$\hat{X} = \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \\ \hat{x}_3 \\ \hat{x}_4 \end{bmatrix} = \begin{bmatrix} \frac{A}{\Psi} - \frac{D}{\Lambda} \\ \frac{B}{\Psi} + \frac{C}{\Lambda} \\ \frac{C}{\Psi} + \frac{B}{\Lambda} \\ \frac{D}{\Psi} - \frac{A}{\Lambda} \end{bmatrix} \tag{11}$$

where

$$\begin{aligned} \Psi &= \alpha\left(1 - \frac{\beta^2}{\alpha^2}\right) \\ \Lambda &= \frac{\alpha^2}{\beta}\left(1 - \frac{\beta^2}{\alpha^2}\right) \end{aligned} \tag{12}$$

By re-introducing the contribution of the Noise (renaming $H^H N = W$) and relating the decoded vector $\hat{X}$ to the transmitted symbol, it is possible to obtain:

$$\hat{X} = \frac{1}{\alpha} X + \frac{1}{\alpha} \begin{bmatrix} \frac{w_1}{\Psi} - \frac{w_4}{\Lambda} \\ \frac{w_2}{\Psi} + \frac{w_3}{\Lambda} \\ \frac{w_3}{\Psi} + \frac{w_2}{\Lambda} \\ \frac{w_4}{\Psi} - \frac{w_1}{\Lambda} \end{bmatrix} \tag{13}$$

This methodology allows decoding a STBC transmitted signal in a more stable way compared to the channel inversion, given the fact that the estimated channel matrix is never directly inverted during the process. It is of course true that the noise contribution can become significant, if the noise levels of the adopted receiver technology are too high. Nevertheless, such levels are supposed to be fairly low in systems like WiMAX, which is the one used in this paper to validate the selected multi-antenna methodologies.

3.4 Multiple Input Multiple Output 4x4 case

Let us now assume a full blown 4x4 MIMO system as depicted in Fig.3.

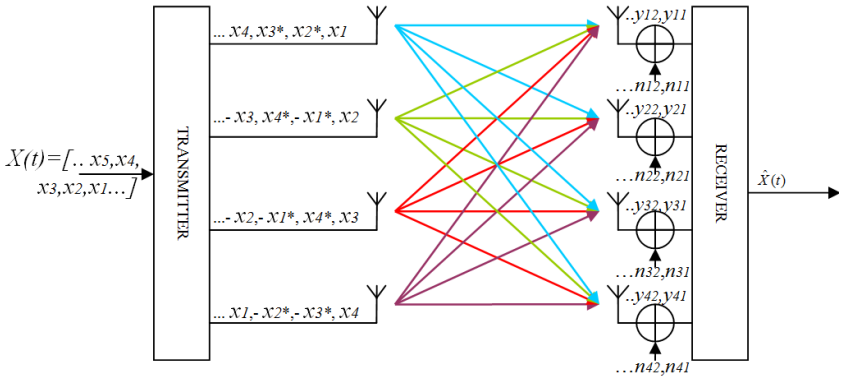


Figure 3. MIMO 4x4 case: the transmitter at the left side exploits an extended Alamouti STBC transmission while a combiner at the receiver (right) side attempts to decode the transmitted streams. Spatial diversity exploits here the full potential due to the presence of 4 receiving antennas.

The MIMO channels are shown in four colors to illustrate how to split them into four groups. The choice of a 4x4 MIMO instead of the usual 2x1 or 2x2 configurations is motivated by the necessity of increasing diversity in the space domain (and therefore robustness against fading effects) together with the spectral efficiency. Nowadays, a 4-element MIMO array can be implemented with affordable cost and the yielded performance improvement in terms of spectral efficiency may justify such an additional (non-prohibitive) cost even at the terminal side.

The signal received during a MIMO symbol period is given as follow [20]:

$$Y = HX + N \tag{14}$$

where H denotes the non-squared channel matrix composed of 16 rows and 4 columns, X the 4x4 Alamouti STBC matrix containing the space-time encoded OFDM symbols as seen in Equation (2), and finally N the noise matrix, made of independent and identically-distributed Gaussian noise samples.

3.5 Channel Pseudo-Inversion Combiner

As the channel matrix is not square, the direct matrix inversion cannot be employed in order to perform the space-time combining at the receiver side. However, the pseudo-inversion can be computed [20] even for a non-squared matrix by using:

$$H^{+} = (H^{T}H)^{-1} \tag{15}$$

That leads to:

$$\tilde{X} = H^{+}Y = H^{+}HX + H^{+}N = X + H^{+}N \tag{16}$$

However, the computation of the pseudo-inverse is computationally expensive, since it includes a matrix inversion involving a 16x16 matrix; this is especially true when implementing the method in hardware. Furthermore, the performance may degrade due to the increase of the noise level generated by the multiplication of the noise matrix by the pseudo-inverse channel matrix. It still anyway holds the ill-positioning of this type of solution.

3.6 Subtractive Combiner

It is possible to easily extend the Subtractive combiner presented for the 4x1 case and use it as a computationally lighter decoding technique. This fits particularly with the goal of the hardware implementation of the method.

As a matter of fact, the channel matrix, which has now dimension 16x4, when combined with the Hermitian channel matrix produces a similar output compared to the 4x1 MISO case. The only difference resides in the definition of the α and β used in the technique:

$$\begin{aligned}\alpha = {} & |h_{11}|^2 + |h_{12}|^2 + |h_{13}|^2 + |h_{14}|^2 + |h_{21}|^2 + |h_{22}|^2 + |h_{23}|^2 \\ & + |h_{24}|^2 + |h_{31}|^2 + |h_{32}|^2 + |h_{33}|^2 + |h_{34}|^2 \\ & + |h_{41}|^2 + |h_{42}|^2 + |h_{43}|^2 + |h_{44}|^2\end{aligned} \tag{17}$$

and

$$\beta = 2 \cdot Re(h_{11}^{*} h_{41} - h_{21} h_{31}^{*} + h_{12}^{*} h_{42} - h_{22} h_{32}^{*} + h_{13}^{*} h_{43} - h_{23} h_{33}^{*} + h_{14}^{*} h_{44} - h_{24} h_{34}^{*}) \quad (18)$$

In order to obtain the decoded values, the same methodology shown in equations from (9) to (13) has to be applied, with the exception of the different multiplicative factors derived in (17) and (18). The usage of this technique allows reducing the number of operations due to the computation of the pseudo-inverse channel matrix and provides more stability since no inversion is applied. It still holds the note that the noise levels need to be properly evaluated before applying this technique.

3.7 Comparative Overview

The two different algorithms described above, i.e. channel pseudo-inversion and subtractive combining have been tested by means of intensive simulation trials in the Matlab-Simulink environment and the simulation results are shown in Fig.4. The IEEE 802.16-2004 system of Fig.1 has been simulated over a Rayleigh fading MIMO channel, characterized by a delay spread of 1 μs. and Doppler spread 0.5 Hz, which correspond to a typical urban environment with no terminal mobility. The simulation results are related to 100 average trials for each signal-to-noise ratio values. Given the extremely reduced number of simulated samples, what is relevant for the investigation is the trend of the results more than the absolute value obtained.

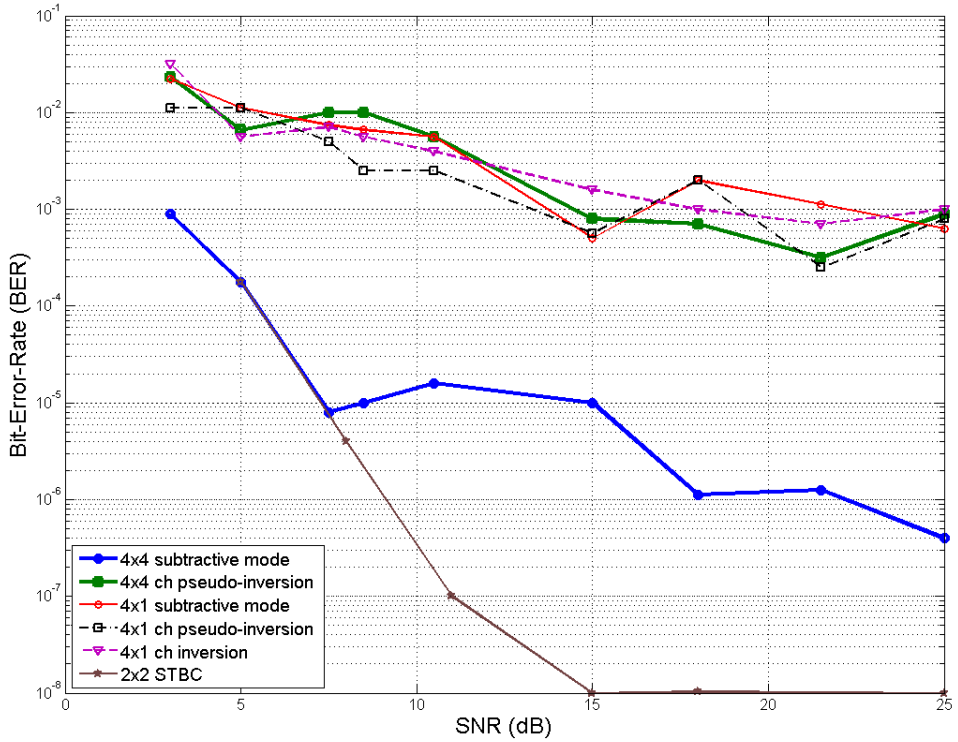


Figure 4. Comparative result generated through Matlab-Simulink simulation: as expected the 2x2 MIMO is the more robust given the reduced number of antennas. The 4x1 methodologies and the 4x4 channel pseudo-inversion are comparable in terms of performance. The increased spectral efficiency is paid in terms of robustness.

The comparison in terms of robustness with the 2x2 traditional STBC shows that with high SNR values the 4x4 method is less robust. This is of course due to the presence of more "interferers" (more antennas). It has to be reminded that the transmission methodology is fairly simple and it has no feedback-based precoding in order to avoid interference on the channel. In the 4x1 case the subtractive combiners does not provide a clear gain since the receiver cannot exploit the spatial diversity due to the presence of one antenna only.

As a matter of fact Fig.4 presents some absolute numbers which are not fully consistent, given the reduced number of simulation samples. Nevertheless, it is clear from the trend that subtractive combining provides much better results with a reduced computational burden. The advantage is, of course, clear when multiple antennas are available. For this reason, we decided to select this solution for the practical SDR-based implementation.

4. OFDM-STBC Implementation on FPGA

There are several valuable approaches to implement the subtractive combiner presented in Section 3. In this paper, an efficient solution from a computational viewpoint is presented. The architecture is designed by considering a cost function based on the execution time and the FPGA resources parameters. Finding a suitable solution is a matter of trading off these two parameters. The proposed solution exploits the maximum operation parallelism in order to reduce the execution time. On the other hand, to minimize the number of required resources, basic real operators are used, such as multipliers, adders, and CORDIC dividers [21]. Moreover, the use of integrated processors and high accuracy operators is avoided to preserve the initial trade-off.

The inputs of the system are the received signal matrix Y and the estimated channel matrix H. All the signals are complex variables, so real operators must be combined to perform this operation. This is done minimizing the number of operators, such as avoiding complex divisions (which would need a large amount of resources), replacing them with complex multiplications followed by real divisions.

The architecture includes the parallel operators which compute the decoding operation with the coefficients α and β of (17) and (18). The final outputs are the interference-free decoded OFDM symbols obtained by solving the linear system of (11) but extended for the 4x4 case. In order to evaluate the implementation of the subtractive 4x4 OFDM-MIMO combiner considered in this paper, a Xilinx Virtex 5 xc5vsx50t-1ff1136 FPGA has been used. For the specification, synthesis, and implementation, System Generator and Xilinx ISE have been used.

The OFDM-MIMO main scheme shown in Fig.1 has been adapted to provide the 4x4 transmission data to the MIMO combiner which has been implemented by means of System Generator.

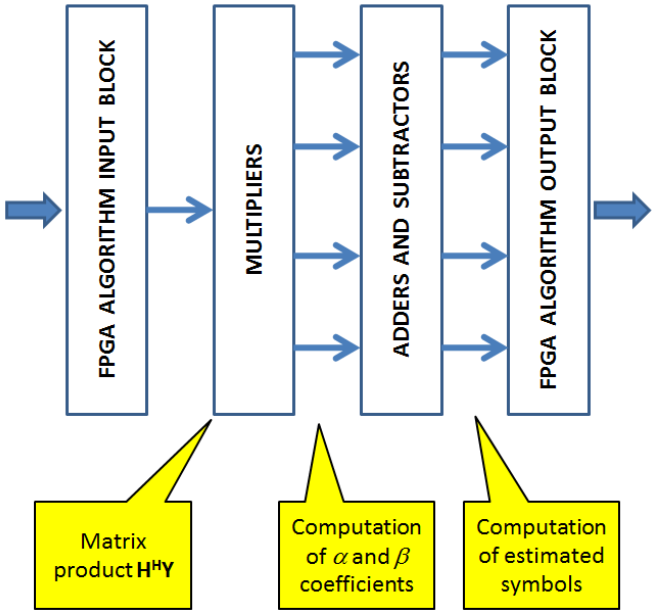


Figure 5. The STBC 4x4 subtractive combiner scheme which has been implemented in SysGen blocks.

In Fig.5 the architecture of the implementation is shown. The inputs are the received signals coming from the 4-antennas OFDM receivers, and the MIMO channel estimations. In order to allow the interface between System Generator and Standard Matlab blocks, the signals must be split from floating point complex values into real-imaginary parts. Note that here the System Generator input ports reduce the accuracy to 8-bit. This choice is due to the limited number of available I/O ports (480) and of slices in the FPGA. Moreover, note that the full amount of I/O ports is used with the aim of parallelizing the architecture, and thus it is necessary to avoid serial inputs.

In Fig.6 the corresponding SysGen diagram of the subtractive combiner is shown.

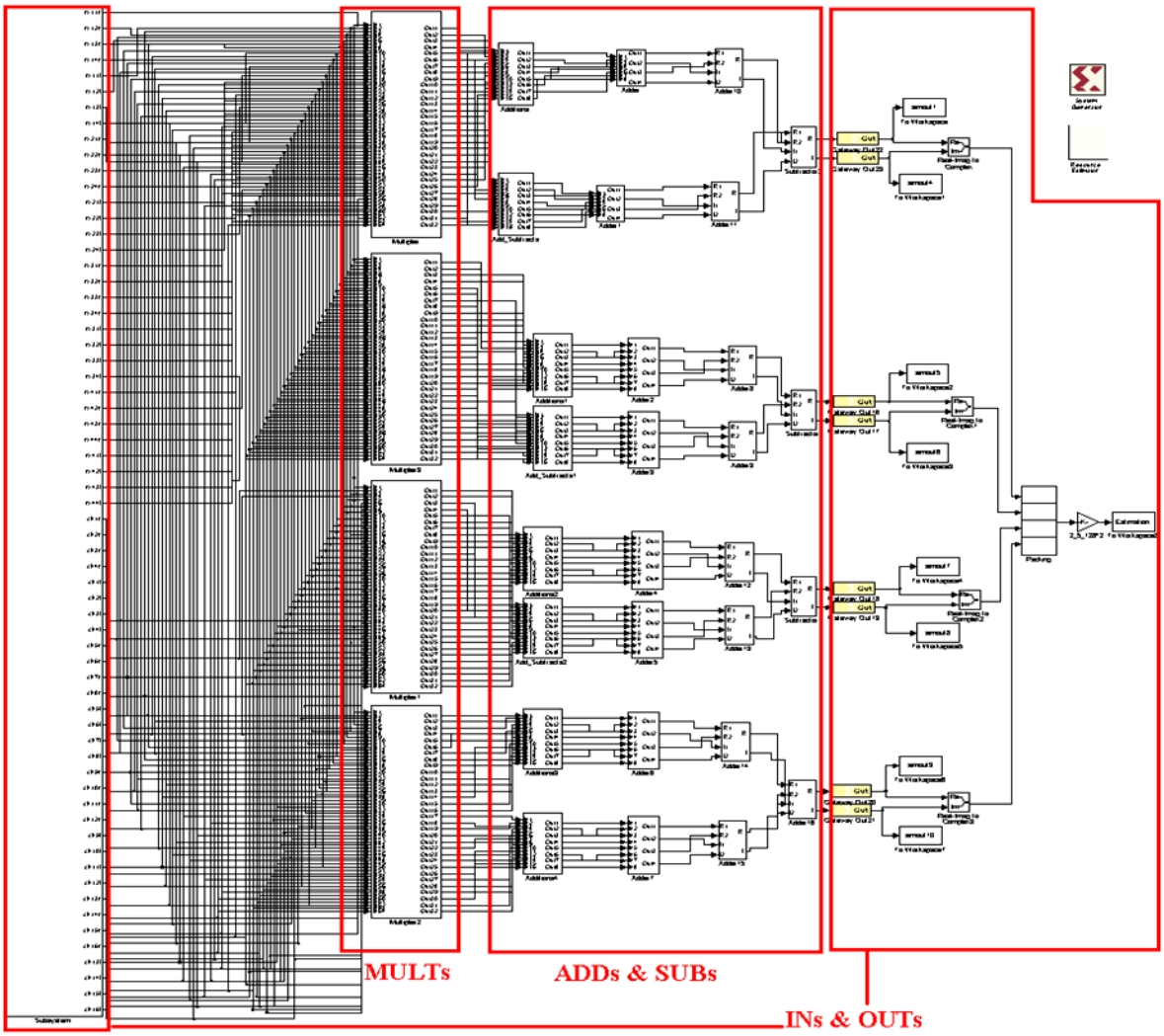


Figure 6. The STBC 4x4 subtractive combiner (SysGen diagram).

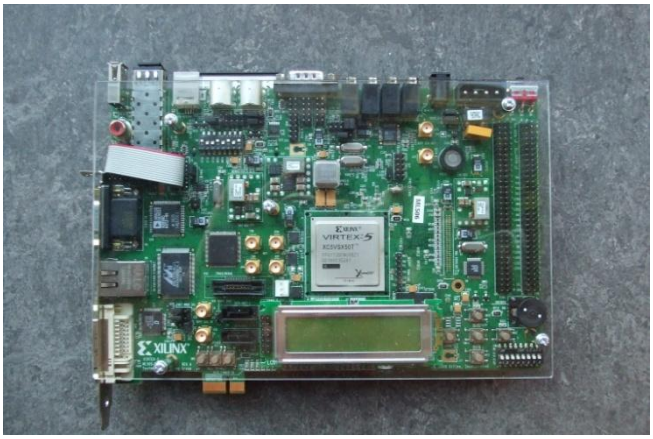
The banks at the top of Figure 6 execute the matrix product between the received signal and the channel estimation. The operators used here maintain the 8-bit accuracy and their delays are set to exploit a pipelined cascade. The weighs for the interference cancellation are implemented by the blocks on the bottom of Fig. 6. Finally, the two parts computations are combined to obtain the final symbol estimation.

5. Experimental results

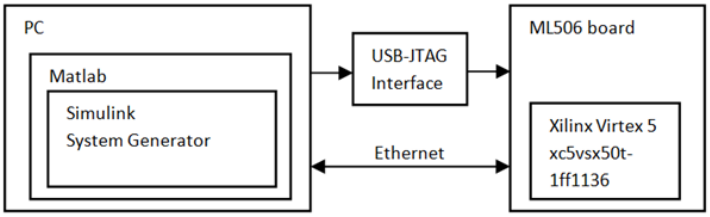
The System Generator MIMO combiner is synthesized and the generated bitstream file is loaded on the FPGA. In order to manage the system in real time, a HW/SW co-simulation environment is set. The data transmitted from the computer to the FPGA are serialized by a point-to-point Ethernet

connection. This testing environment allows a direct comparison between the software and the FPGA results.

The 4x4 MIMO decoder has been specified in Simulink via Xilinx System Generator and the corresponding HDL code has been generated with the same tool. Then, the design has been synthesized, placed, and routed using Xilinx ISE. Finally, the bistream file has been generated using the same tool.



(a)



(b)

Figure 7. (a) ML506 board picture, (b) co-simulation setup scheme

In Fig.7 the used FPGA evaluation board (a) and the co-simulation setup scheme (b) are shown.

The HW/SW co-simulation is supported by the following tools:

- MATLAB version 7.6.0.324 (R2008a);
- SIMULINK 7.1.1. (R2008a+);
- Xilinx ISE Design Suite 11.1 (including System Generator for DSP 11.1);
- ML506 board with a Virtex 5 xc5vsx50t-1ff1136 (see Fig.5a);
- Ethernet cable (for the HW/SW co-simulation);

- USB-JTAG cable (for programming the FPGA);
- Power supply;
- Computer from the Embedded Systems Laboratory of the Department of Electronic Systems, AAU (2 GHz single core, 1 GB RAM).

In Fig.8, a snapshot of the synthesis results is shown; looking at the numbers it is possible to conclude that the design fits into the targeted FPGA, with 57 % of area occupation (slices). The most critical value, as expected, is the number of bonded I/Os, which is at 80% of utilization. This could be problematic if the hardware implementation should be extended. The number of DSP48E embedded multipliers is at 88 % but it is not so critical, because the multipliers can be implemented also by standard slices (of which ca. 40% are still available), so the number of multipliers can be reasonably incremented.

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	464	32,640	1%
Number of occupied Slices	4,688	8,160	57%
Number of LUT Flip Flop pairs used	13,965		
Number used as logic	13,136	32,640	40%
Number used as Memory	128	12,480	1%
Number of bonded IOBs	385	480	80%
Number of DSP48Es	256	288	88%
Number of BUFG/BUFGCTRLs	1	32	3%

Figure 8. Snapshot of the results of the synthesis. The resources considered are the number of slice/slice registers, Flip-Flops, Memory usage, bits of I/Os, Embedded multipliers (DSP48E) and Buffers.

Another typical parameter is the working frequency of the system on FPGA. The co-simulation generation tool allows using a 10 ns FPGA clock period, the maximum available in System Generator for the given FPGA board.

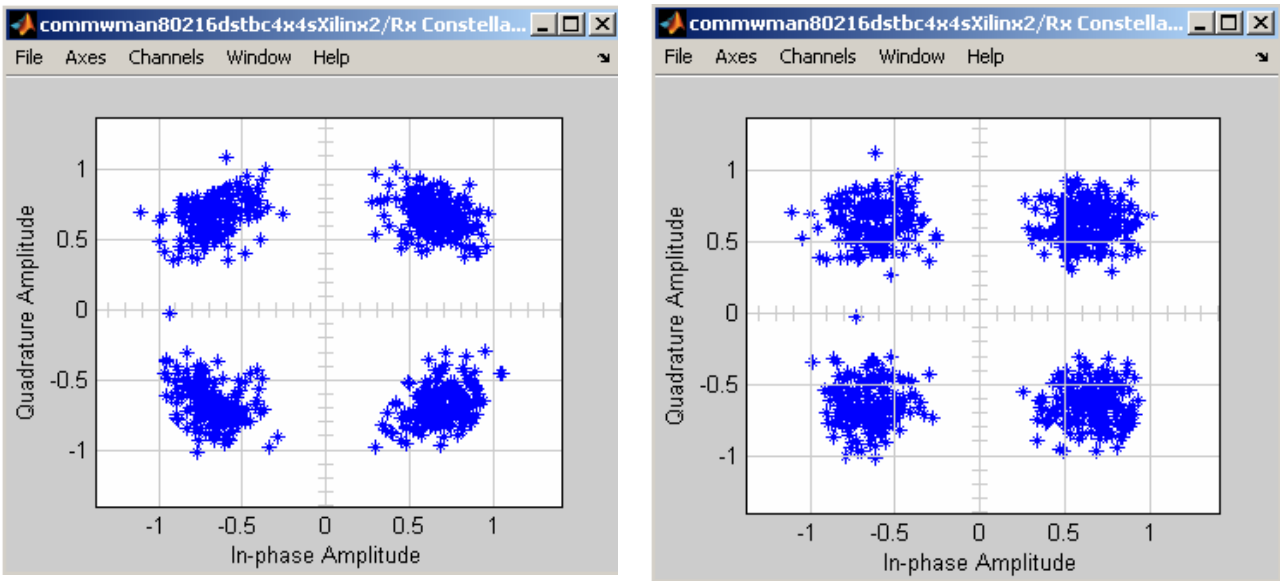
The longest path of the system implemented on FPGA falls within the allowed limit:

- FPGA clock period (co-simulation) = 10 ns;
- Longest path = 9.986 ns.

The time slack, i.e. the difference between the longest available period (here 10 ns) and the required period for the design (here 9.986 ns) is just 14 ps, which means that it is most likely impossible to cascade other combinatorial operators without introducing intermediate registers.

Regarding this point, it can be useful to analyze the trade-off between latency and delay. The latency is the time needed to complete a cascade of combinatorial operations (in this case equal to the longest path). The delay is the additional time introduced by sequential elements (as registers). By analyzing this trade-off, it could be possible to reduce the total execution time, depending on the targeted application and its constraints.

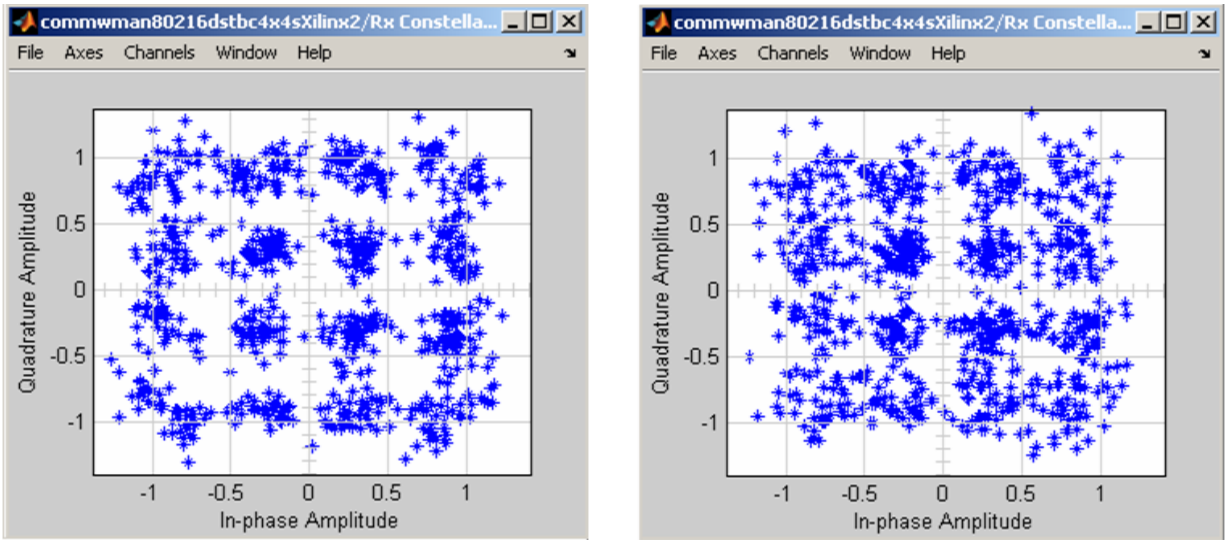
Another aspect that has to be taken into account is the accuracy reduction due to the decrement from 64 bits values used in the Simulink simulations and the 8 bits precision used instead in the hardware.



(a) (b)

Figure 9. Visual comparison between a (a) 64bits received constellation (after the software combiner) and a (b) 8bit received one (after the hardware combiner) for a QAM modulation. The constellations have been obtained by processing the same exact bursts.

In Figure9 a visual comparison of the precision differences for a QAM case are shown. A similar comparison has been performed also for the 16-QAM case, as shown in Figure 10.



(a) (b)

Figure 10. Visual comparison between a (a) 64bits received constellation (after the software combiner) and a (b) 8bit received one (after the hardware combiner) for a 16-QAM modulation. The constellations have been obtained by processing the same exact bursts.

In order to provide more significant results, 200 co-simulations have been performed and the results are shown in Table 1.

Table 1. Mean relative errors in the received constellations due to the reduction of the accuracy from 64bits to 8 bits.

Modulation/error	**Mean Relative Error for Real part**	**Mean Relative Error for Imaginary part**
QAM	8,68%	8,72%
16-QAM	14,2%	14,4%

The mean relative error shown in Table 1 has been computed by averaging the difference, for each burst, between the signal processed by the Simulink 64 bits implementation and the 8 bits SysGen one and normalized respect to the 64 bits signal.

As expected the reception of the 16-QAM is more affected by the reduction in the data precision. Nevertheless, the evidenced order of magnitude emphasizes the fact that this aspect cannot be neglected while comparing the performances of a hardware-developed method with the simulation ones.

6. Conclusions and future works

This paper proposes an optimized implementation of a 4x4 decoder for OFDM-MIMO systems by means of a rapid prototyping approach for FPGA. The innovative design allows reducing the execution time and preserving the number of resources, as compared to other state-of-the-art implementations. The parallel computation allows minimizing the clock period and the pipelining of the operations. The final results illustrate that a FPGA-based hardware implementation is feasible. The proposed solution could also be implemented on ASIC or DSPs (in that case the clock frequency/execution time/resource usage would be different as compared to the FPGA implementation); moreover, the proposed solution allows a possible scalability of the system for instance by increasing the number of antennas.

References

[1] L. Hanzo, Y. Akhtman, L. Wang, and M. Jiang, *"MIMO-OFDM for LTE, WiFi and WiMAX: Coherent versus Non-coherent and Cooperative Turbo Transceivers"*, Wiley – IEEE Press, 2011.

[2] D. Gesbert, M. Shafi, et. al., "From Theory to Practice: An Overview of MIMO Space-Time Coded Wireless Systems", *IEEE J. Sel. Areas in Comm.*, vol. 21, no. 3, Apr. 2003, pp. 281-301.

[3] S.M. Alamouti, "A simple transmit diversity tecnique for wireless communications", *IEEE J. Sel. Areas in Comm.*, vol.16, no. 8, Oct. 1998, pp. 1451-1458.

[4] G.J. Foschini, "Layered Space-Time Architecture for Wireless Communication in a Fading Environment when using Multi-Element Antennas", *Bell Labs Tech. Jour.*, vol. 1, no.2, pp. 41-59, 1996.

[5] R.V. Heath, and A.J. Paulraj, "Switching between Diversity and Multiplexing in MIMO Systems", *IEEE Trans. on Comm.*, vol.53, no.6, June 2005, pp. 962-968.

[6] Y.Q. Bian, A.R. Nix, E. Tameh, and J. McGeehan, "MIMO-OFDM WLAN Architectures, Area Coverage and Link Adaptation for Urban Hotspots", *IEEE Trans. on Vehicular Tech.*, vol.57, no.4, July 2008, pp. 2364-2374.

[7] J. Chung, Y. Yun, and S. Choi, "Experiments on MIMO-OFDM system combine with adaptive beamforming based on IEEE 802.16e WMAN standard", *Telecommun Syst,* published online 4 June 2011, DOI 10.1007/s11235-011-9475-7, pp. 1-14.

[8] T. Aruna, and M. Suganthi, "Variable power adaptive MIMO OFDM system under imperfect CSI for mobile ad hoc networks", *Telecommun Syst*, published online 12 Aug. 2010, DOI 10.1007/s1235-010-9387-y, pp. 1-7.

[9] A. Gupta, A, Forenza, and R.W. Heat, "Rapid MIMO-OFDM Software Defined Radio System Prototyping", *Proc. of 2004 IEEE Workshop on Signal Processing Systems (SIPS 2004)*, Austin (TX), 13-15 October 2004, pp. 182-186.

[10] X. Li, W. Hu, H. Yousefi'zadeh, and A. Qureshi, "A Case Study of a MIMO SDR Implementation", *Proc. of IEEE MILCOM 2008 Conf.*, San Diego (CA), 16-19 Nov. 2008, pp.1-7.

[11] M. Palkovic, H. Capelle, M. Glassee, B. Bougard, and L. Van der Perre, "Mapping of 40 MHz MIMO SDM-OFDM Baseband Processing on Multi-Processor SDR Platform", *Proc. of 11th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2008)*, Bratislava (SK), 16-18 Apr. 2008, available on CD-ROM.

[12] H.K. Pan, J. Tsai, S. Golden, V.K. Nair, and J.T. Bernhard, "Reconfigurable Antenna Implementation in Multi-radio Platform", *Proc. of IEEE Antennas and Propagat. Symp. (AP-S 2008)*, San Diego (CA), July 5-11, 2008, CD ROM available.

[13] C. Thomos, and G. Kalivalas, "FPGA-based architecture and implementation techniques of a low-complexity hybrid RAKE receiver for a DS-UWB Communication System", *Telecommun Syst*, published online: 02 June 2011, DOI 10.1007/s11235-011-9487-3, pp. 1-15.

[14] S. Haene, D. Perels, and A. Burg, "A Real-Time 4-Stream MIMO-OFDM Transceiver: System Design, FPGA Implementation and Characterization", *IEEE Journal on Selec. Areas in Comm.*, vol. 26, no. 6, August 2008, pp. 877-889.

[15] J. Wang, and G.E. Sobelman, "Joint MIMO transceiver design based on uniform channel decomposition", *Electronics Letters*, vol. 47, no. 5, 3rd March 2011, pp. 1-2.

[16] S. Yu, T.H. Im, C.H. Park, J. Kim, and Y.S. Cho, "An FPGA Implementation of MML-DFE for Spatial Multiplexed MIMO Systems", *IEEE Trans. on Circuit and Systems – II: Express Briefs*, vol. 55, no. 7, July 2008, pp. 705-709.

[17] L. Boher, R. Rabineau, and M. Helard, "FPGA Implementation of an Iterative Receiver for MIMO-OFDM Systems", *IEEE Journal on Selec. Areas in Comm.*, vol. 26, no. 6, August 2008, pp. 857-866.

[18] X. Huang, C. Liang, and J. Ma, "System Architecture and Implementation of MIMO Sphere Decoders on FPGA", *IEEE Trans. on VLSI Systems*, vol. 16, no. 2, February 2008, pp. 188-197.

[19] IEEE Standard 802.16-2004, "*Part 16: Air interface for fixed broadband wireless access systems"*, October 2004, http://ieee802.org/16/published.html.

[20] T. Kaiser, A. Bourdoux, et. al. (eds.) "Smart Antennas – State of the Art", *EURASIP Series on Signal Processing and Communications*, Hindawi: 2005.

[21] J. E. Volder, "The CORDIC Trigonometric Computing Technique", *IRE Trans. On Electronic Computers*, Vol. EC-8, 1959, pp. 330-334.