A clock-less PWM architecture for sensor imaging

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***Abstract*—In this paper, a novel image sensor architecture based on a clock-less readout is presented. The proposed proof-of-concept consists of only 12x6 pixels and validates the new readout scheme designed for low power application, which is particularly suitable for embedding energy harvesting circuit even though not included into the design. Thanks to the clock-less serial readout with embedded PWM interface, the sensor delivers still images at maximum 1Kfps showing a dynamic range of at least 72 dB. A typical value of power consumption of the entire array is estimated about 35nW at 1.6V of power supply.**

Keywords—low-power imaging, energy harvesting, PWM

I. INTRODUCTION

Wireless sensor nodes can be used to monitor environmental parameters in a wide area. Among different types of sensor nodes, video nodes have to deal with image cameras, which usually show higher complexity in term of data processing and power request with respect to single detectors such as light, temperature or pressure sensors. Because of the need to extend the life-time of each node, the use of ultra-low power imagers is of crucial importance. It is possible to find in the literature different techniques aimed at lowering the power consumption, such as reconfigurable architectures [1], smart sensors [2-3], ultra-low voltage architectures [4] and imagers with energy harvesting [5-8]. These last detectors exploit the pixel photodiode as a source of energy for the sensor itself working in a similar way as a tiny solar cell. Specifically, authors in [5] first introduced the concept of self-powered cameras. The proposed approach uses two photodiodes per pixel: one fully dedicated to energy harvesting (a p+/nwell) and one for signal readout (a n+/P-sub). The presence of two photodiodes into the pixel reduces the pixel fill factor, while a standard readout scheme was used for image acquisition. Publication in [6] proposed an array of 4x4 pixels with dual harvesting photodiodes for generating power supplies of the sensor. An address event architecture was designed for the pixel readout. The main drawback of this architecture is the scalability to larger sensor resolution. An interesting example of imager with embedded energy harvesting capability is shown in [7] where a standard 4T pixel with two stacked photodiodes (a n-well/p-sub for imaging mode and a p+/n-well for harvester) is proposed. The idea introduced in [7] is to use a single reconfigurable photodiode per pixel, in order to maximize the pixel fill factor. As consequence, the photodiode can be used in imaging or in energy harvesting mode. Nevertheless, during the image acquisition the energy harvesting circuit can not work. Papers in [10-11] try to overcome this issue by configuring the array of pixels in such a way that part of them will be devoted to energy harvest, part of them to image acquisition, with consequent loss of resolution. Alternatively, paper in [9] uses an asynchronous mode (first to time approach) or current mode [8] to readout the pixel.

In the present paper, we propose a new architecture, specifically designed for enhancing the energy harvesting capability of the sensor without affecting the image resolution. In order to further reduce the power consumption of the chip, this paper proposes a new readout technique, allowing to perform the analog to digital conversion of the light at the pixel level. The proof-of-concept here presented aims at demonstrating the functionality and performance of the new architecture while the harvesting part will be embedded into a new sensor design.

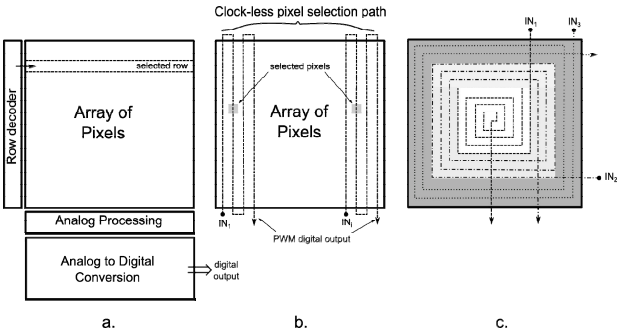

Figure 1: New sensor architecture

The paper is organized in this way: Section II describes the principle of the new readout technique while Section III describes the pixel schematic in detail. Section IV gives some measurement results after sensor characterization.

II. NEW ARCHITECTURE

In video node systems, the power consumption requirement of the camera and the capability to deal with high dynamic range scenes have higher priority than the image performance in term of sensor resolution, frame rate or noise. As a consequence of this, the design of an ultra-low power camera has to be a good trade-off between power consumption and image quality. In particular, considering camera speed, in some applications the user does not need to work at high frame rates, but still images with low refresh rate can be enough to understand scene changes. The low power sensor proposed here favors the efficiency of the readout circuit in terms of

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power and dynamic range, but, at the same time, reduces the overall sensor speed.

The idea of the proposed architecture is shown in Figure 1b and Figure 1c. The array does not have conventional horizontal and vertical decoders for pixel addressing nor analog processing and ADC at column level for pixel readout (see Figure 1a), being able to execute these operations at the pixel level. The sensor can work in two modalities: harvesting mode and imaging mode. During the harvesting mode, all photodiodes are configured to harvest the photo-generated current. During the imaging mode, the sensor uses a clock-less scanning circuit which, following a hardwired path, sequentially reads every pixel. Each pixel, when selected, starts integrating the light and, at the same time, converts this value in digital domain. In this scheme, when one pixel is readout, all others are still working in harvesting mode, thus partially recovering the energy used for the conversion. In case of high resolution imagers, in order to increase the frame rate of the sensor, multiple readout paths can work in parallel, as shown in Figure 2b. In this case, the number of pixels selected for image readout are proportional to the number of implemented readout paths. The hardwired readout circuit can follow different paths. For example, the architecture depicted in Figure 2c shows a possible implementation of a special sensor where different scanning circuits are devoted to the acquisition of specific sensor areas. In particular, the central part of the sensor can be separately readout form the periphery one, thus identifying a region of interest.

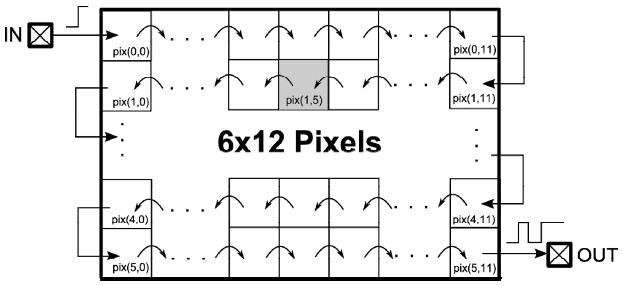

Figure 2: Sensor implemented into the fabricated chip

The present paper describes the design and the characterization of a small proof-of-concept device, consisting of only 6x12 pixels (see Figure 2) without energy harvesting capability to demonstrate the readout circuit functionality. In normal operation, all pixels of the sensor are under reset and the overall photo generated current is sourced by the reset voltage V_{res} (IN=L). During image acquisition (IN=H), pixels are sequentially scanned following a snake-shaped path, hardwired into the array as shown in Figure 2. The positive edge of the input signal IN is propagated from the first pixel, in position (0,0), to the last one, in position (5,11), through each row of the array, thus implementing a clock-less scanning circuit. Every pixel is then connected to the previous pixel and to the next one through digital signals in order to form a chain (see Figure 4). When the propagating signal reaches a pixel, as for example the pixel in position (1,5) in Figure 2, an analog to digital conversion is performed during the integration time.

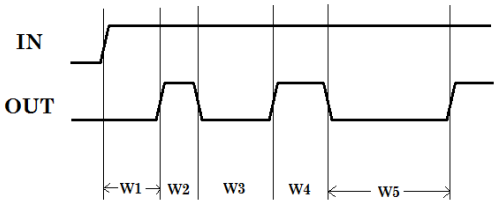

Figure 3: Typical readout timing diagram.

The timing diagram of Figure 3 shows a typical waveform generated at the output of the sensor. While the positive edge of the input signal (IN) is propagating through the sensor, the output (OUT) generates a digital pattern, coding the analog value of the pixels. In particular, the measurements of the distance between two consecutive edges of OUT, i.e. W1, W2 and W3 of Figure 3, are inversely proportional to the value the light impinging on pixels of Figure 2 in position (5,11), (5,10) and (5,9) respectively. Please note that in this modality every transition of OUT will generate a new pixel value, thus halving the number of output transitions and optimizing the power consumption of the chip for data delivery.

III. PIXEL TOPOLOGY

The pixel schematics is shown in Figure 5. It consists of 20 transistors per pixel and a large n-well photodiode in order to guarantee enough energy scavenging. The pixel has been realized in a standard CMOS 0.35µm technology and shows a squared area of 30x30um^2 with 41% of fill factor.

As shown in Figure 5, the pixel consists of a smart reset circuit of the photodiode, followed by a low-power comparator and by a PWM generator. Pixels are connected to each other forming a chain as shown in Figure 4. At the initial state, the IN signal is low and all pixels are under reset (harvest mode) while signal SIGin is forced to gnd for initializing the network. In this condition, internal node Vph is set to Vref, while the comparator is under reset, meaning that COUT is forced to vdd and Vf to gnd.

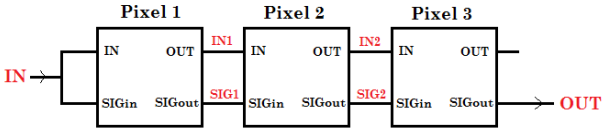

Figure 4: Connection among pixels into the array. The propagation of signal OUT and SIGout forms a chain for sensor readout.

Whenever it is required to read an image, signal IN is set to high. As a consequence of this operation, the smart reset circuit switches off transistor Mp1, disconnecting the photodiode to Vres and leaving the Vph node floating.

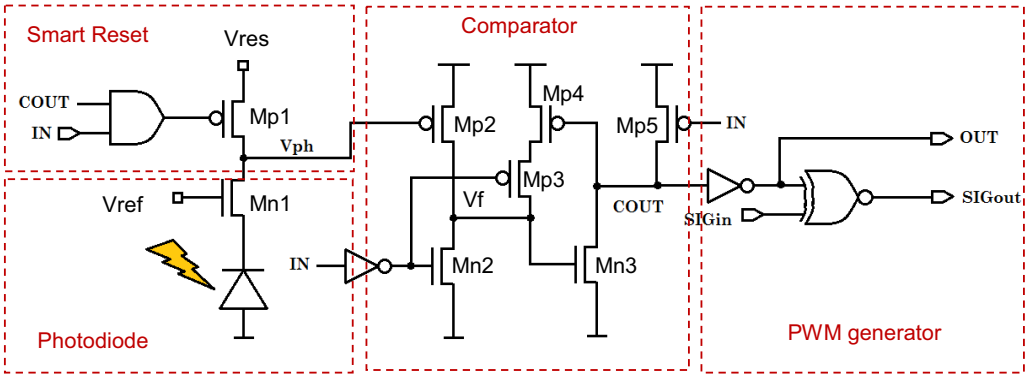

Figure 5: Pixel schematic

Transistor Mn1, biased at a fixed voltage Vref, allows increasing the output impedance of the circuit, speeding up the integration of the impinging light on node Vph. In this phase, the first pixel of the array is integrating the light while all others are still under reset (or in harvest mode). In the meantime, the comparator, previously reset, is now ready to compare the input signal: transistor Mn2 and Mp3 are switched off, while Mp5 is forced to be on.

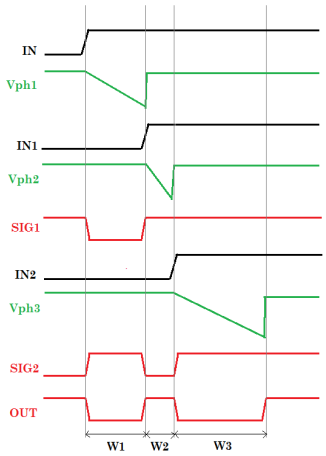

Figure 6: Timing diagram of the pixel during the readout phase.

During the integration time, the acquired photocurrent discharges the Vph node until the voltage threshold of the comparator. This intrinsic threshold is set equal to Vdd-Vth_{Mp2} where Vth is the voltage threshold of Mp2. The core of the comparator consists of transistors Mn3 and Mp4 forming a positive feedback in order to improve the speed of the comparison. As soon as Mp2 start conducting, the comparator toggles and the output node COUT is fast pulled down. The output of the comparator is then connected to the following pixel to guarantee the signal propagation, and to the PWM circuit to change the state of SIGout. As shown in Figure 5, the presence of the XNOR gate allows to change the state of SIGout every time a comparator triggers. In this readout modality the total readout time will be equal to the sum of the integration time of every pixel, thus imposing the need of multi-readout paths in a large sensor resolution to increase the frame rate.

IV. Experimental Results

The small prototype has been tested in the lab in order to verify its functionality. In particular, the device has been connected to an FPGA for both controlling the sensor and acquiring the output signal. The PWM signal is converted by means a 16 bit counter working at 50MHz. The signal is then visualized by means of a program in python to have a rough estimation of the image quality.

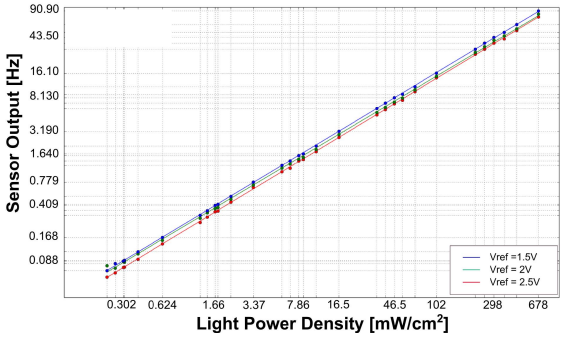

Figure 7: Output frequency of the pixel versus light power density variation.

Figure 8: Example of image acquired by the sensor (without averaging)

The response of the chip versus the increase of light was first measured, considering an average among 10^3 acquired frames. The result of this measurement is shown in Figure 7 where the different curves are related to different bias conditions of the pixel. The trend of the output frequency can

be considered, in first approximation, linear. The dynamic range of the sensor has been measured to be at least 72dB and limited by the present setup.

The FPN of the sensor has been extracted for every point of Figure 7. The value of FPN is almost constant versus light variation and estimated equal to about 15%. This value of FPN could be partially due to the mismatch of the readout circuit, implemented at the pixel level, and partially due to boundary effects, which are not negligible in this small array (see Figure 8).

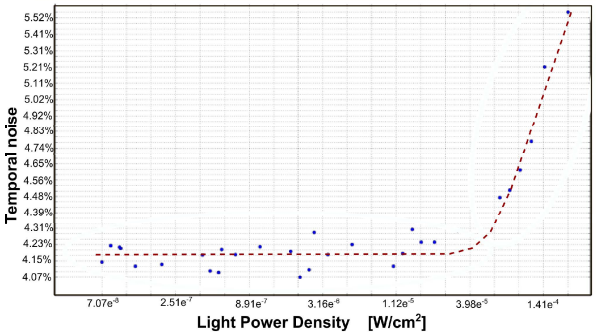

Figure 9: Temporal noise of the pixel.

The pixel temporal noise, calculated as the output jitter of the PWM signal over 10^3 frames, is shown in Figure 9. The temporal noise is almost constant, and equal to about 4.25%, for a quite large range of input light variation (floor noise), while it starts increasing for higher values of light intensity because of the shot noise. The main contribution to temporal noise is the KTC noise of the reset phase, which is not filtered by the implemented circuit.

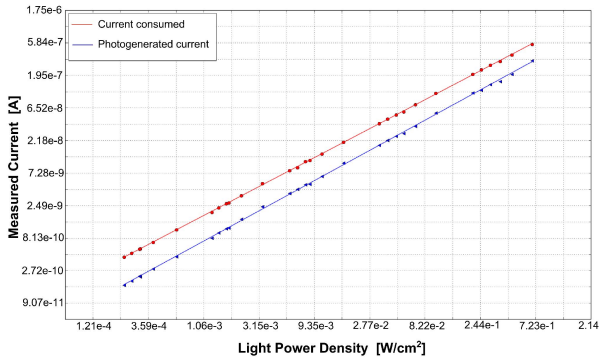

Figure 10: Current consumed by the sensor at different illuminating condition.

The power consumption of the sensor depends on its frame rate. In particular, when the light intensity is high, the frame rate increases and more frames are acquired. In order to show the benefit introduced by the new architecture, the measurement of the current consumed by the sensor activity is compared with the measurement of the photogenerated current flowing through the common node Vref during pixel reset. Figure 10 shows the result of this experiment for different light intensities. From this analysis it is possible to observe that when the light increases, the photo-generated current (blue line) increases more than the current consumption (red line). Taking into account a middle point of the plot, for example at 1mW/cm^2 of light power density, the current consumed by the chip I_{pow} is about 22nA, corresponding to about 35nW at 1.6V of power supply, or to a figure of merit of about 0.5nW/pixel. When considering also the photocurrent extracted by the photodiode I_{ph}, the measured value is about 10nA. Subtracting I_{ph} from I_{pow} we obtain a residual current of about 12nA and a corresponding power consumption of 19.2nW or a figure of merit of 270pW/pixel.

V. Conclusions

We presented a new architecture of image sensor suitable to enhance the energy harvesting capability of the device. The proof of concept here implemented is intended to demonstrate the functionality of the new architecture without the implementation of the harvesting part. The approach implements a pixel-level PWM conversion and delivers every pixel in series using a clock-less architecture through a chain propagation. Our future work will focus on the integration of a reconfigurable photodiode embedding also the energy harvesting modality and the design of a new sensor with increased resolution.

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