

nuXmv: introduction and examples *

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Thi Thieu Hoa Le, Alessandra Giordani for FM lab 2005/14

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- NUXMV is a **new** symbolic model checker developed by **FBK-IRST**.
 - based on the NuSMV model checker
 - project url: <https://nuxmv.fbk.eu/>
 - *the binary of NUXMV is available for non-commercial or academic purposes only!*
- NUXMV allows for verifying
 - *finite-state systems* through state-of-the-art SAT-based algorithms;
 - *infinite-state systems* (e.g. systems with *real* and *integer* variables) through SMT-based techniques running on top of **MathSAT5**;
- NUXMV supports *synchronous* systems;
asynchronous systems are no longer supported!

- `nuxmv -int` activates an interactive shell
- `set/unset` set/unset the value of an environment variable.
(e.g. `set input_file filename` sets the input model)
- `read_model [-i filename]` sets the input model and reads it.
- `go`, `go_bmc`, `go_msat` initialize NUXMV for verification or simulation with a specific backend engine.
- `pick_state [-v] [-a] [-r | -i]` picks a state from the set of initial states.
 - `-v` prints the chosen state.
 - `-r` picks a state from the set of the initial states randomly.
 - `-i` picks a state from the set of the initial states interactively.
 - `-a` displays all state variables (requires `-i`).

- `simulate [-p | -v] [-a] [-r | -i] -k N` generates a sequence of at most `N` transitions starting from the current state.
 - `-p` prints the changing variables in the generated trace;
 - `-v` prints changed and unchanged variables in the generated trace;
 - `-a` prints all state variables (requires `-i`);
 - `-r` at every step picks the next state randomly.
 - `-i` at every step picks the next state interactively.
- `reset` resets the whole system (in order to read in another model and to perform verification on it).
- `help` shows the list of all commands (if a command name is given as argument, detailed information for that command will be provided).
note: option `-h` prints the command line help for each command.
- `quit` stops the program.

- `goto_state state_label` makes `state_label` the current state (it is used to navigate along traces).
- `print_current_state [-h] [-v]` prints out the current state.
 - `-v` prints all the variables.
- `show_traces [-t] [-v] [-a | TN[.FS[:[TS]]]` prints the trace `TN` starting from state `FS` up to state `TS`
 - `-t` prints the total number of stored traces
 - `-v` verbosely prints traces content;
 - `-a` prints all the currently stored traces
- `show_vars [-s] [-f] [-i] [-t] [-v]` prints the variables content and type
 - `-s` print state variables;
 - `-f` print frozen variables;
 - `-i` print input variables;
 - `-t` prints the number of variables;
 - `-v` prints verbosely;

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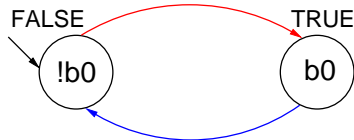
The first SMV program

- an SMV program is composed by a number of **modules**;
- each **module**, contains:
 - state variable declarations;
 - assignments defining the valid *initial states*;
 - assignments defining the *transition relation*;

Example:

```
MODULE main
VAR
  b0 : boolean;

ASSIGN
  init(b0) := FALSE;
  next(b0) := !b0;
```



Basic Types [1/2]

boolean: TRUE, FALSE, ...

```
x : boolean;
```

enumerative:

```
s : {ready, busy, waiting, stopped};
```

bounded integers (intervals):

```
n : 1..8;
```

integers*: -1, 0, 1, ...

```
n : integer;
```

rationals: 1.66, f'2/3, 2e3, 10e-1, ...

```
r : real;
```

words: used to model arrays of bits supporting bitwise logical and arithmetic operations.

- unsigned word[3];
- signed word[7];

*: integer numbers must be within C/C++ INT_MIN and INT_MAX bounds

arrays:

declared with a couple of lower/upper bounds for the index and a type

VAR

```
x : array 0..10 of boolean; -- array of 11 elements
y : array -1..1 of {red, green, orange}; -- array of 3 elements
z : array 1..10 of array 1..5 of boolean; -- array of array
```

ASSIGN

```
init(x[5]) := bool(1);
init(y[0]) := {red, green}; -- any value in the set
init(z[3][2]) := TRUE;
```

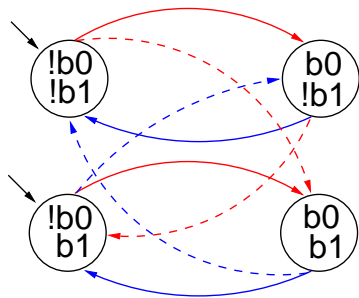
Remarks:

- Array indexes *must be constants*;

Adding a state variable

```
MODULE main
VAR
  b0 : boolean;
  b1 : boolean;

ASSIGN
  init(b0) := FALSE;
  next(b0) := !b0;
```



Remarks:

- the FSM is the result of the **synchronous** composition of the “subsystems” for b0 and b1
- the new state space is the cartesian product of the ranges of the variables.



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set of initial states

is given by the set of states whose variables satisfy **all** the `init()` **constraints** in a module.

```
init(<variable>) := <simple_expression>;
```

- constrains the **initial value** of <variable> to satisfy the <simple_expression>;
- the **initial** value of an **unconstrained** variable can be any of those allowed by its domain;

Example:

```
init(x) := FALSE; -- x must be FALSE  
init(y) := {1, 2, 3}; -- y can be either 1, 2 or 3
```

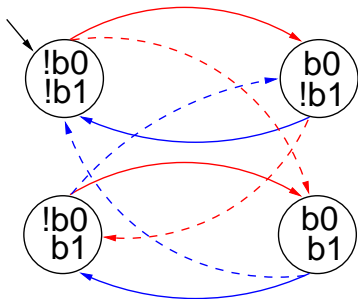
Initial States [2/2]

Example:

```
MODULE main
  VAR
    b0 : boolean;
    b1 : boolean;

  ASSIGN
    init(b0) := FALSE;
    next(b0) := !b0;

    init(b1) := FALSE;
```



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Expressions [1/3]

- arithmetic operators:

+ - * / mod - (unary)

- comparison operators:

= != > < <= >=

- logic operators:

& | xor ! (not) -> <->

- bitwise operators:

<< >>

- set operators: $\{v_1, v_2, \dots, v_n\}$

- **in**: tests a value for membership in a set (*set inclusion*)
- **union**: takes the union of 2 sets (*set union*)

- count operator: counts number of true *boolean* expressions

count(b1 + b2 + ... + bn)

- case expression:

```
case
  c1   : e1;
  c2   : e2;
  ...
  TRUE : en;
esac
```

C/C++ equivalent:

```
if (c1) then e1;
else if (c2) then e2;
...
else en;
```

- if-then-else expression:

```
cond_expr ? basic_expr 1 : basic_expr2
```

- conversion operators: `toint`, `bool`, `floor`, and
 - `swconst`, `uwconst`: convert an integer to a signed and an unsigned word respectively.
 - `word1` converts boolean to a single word bit.
 - `unsigned` and `signed` convert signed word to unsigned word and vice-versa.

- expressions in SMV do not necessarily evaluate to one value. In general, they can represent a set of possible values.

```
init(var) := {a,b,c} union {x,y,z} ;
```

- The meaning of `:=` in assignments is that the lhs can **non-deterministically** be assigned to any value in the set of values represented by the rhs.
- A constant `c` is considered as a syntactic abbreviation for `{c}` (the singleton containing `c`).

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Transition Relation

specifies a constraint on the values that a variable can assume in the *next state*, given the value of variables in the *current state*.

`next(<variable>) := <next_expression>;`

- `<next_expression>` can depend both on “current” and “next” variables:

```
next(a) := { a, a+1 } ;  
next(b) := b + (next(a) - a) ;
```

- `<next_expression>` must evaluate to values in the domain of `<variable>`;
- the **next** value of an **unconstrained** variable evolves **non-deterministically**;

Transition Relation [2/2]

Example:

modulo-4 counter

```
MODULE main
```

```
VAR
```

```
  b0 : boolean;
```

```
  b1 : boolean;
```

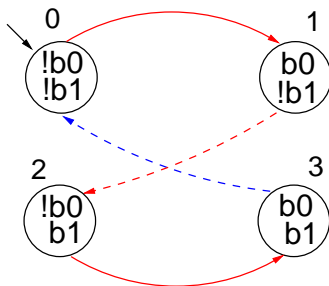
```
ASSIGN
```

```
  init(b0) := FALSE;
```

```
  next(b0) := !b0;
```

```
  init(b1) := FALSE;
```

```
  next(b1) := ((!b0 & b1) | (b0 & !b1));
```



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output variable

is a variable whose value is deterministically depends on the value of other “current” state variables and for which no `init()` or `next()` are defined.

`<variable> := <simple_expression>;`

- `<simple_expression>` must evaluate to values in the domain of the `<variable>`.
- used to model *outputs* of a system;

Output Variable [2/2]

Example:

```
MODULE main
```

```
VAR
```

```
  b0 : boolean;
```

```
  b1 : boolean;
```

```
  out : 0..3;
```

```
ASSIGN
```

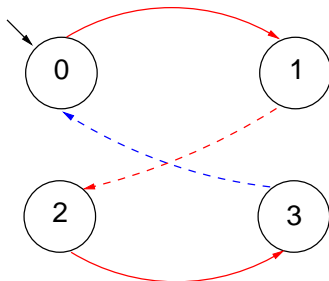
```
  init(b0) := FALSE;
```

```
  next(b0) := !b0;
```

```
  init(b1) := FALSE;
```

```
  next(b1) := ((!b0 & b1) | (b0 & !b1));
```

```
  out := toint(b0) + 2*toint(b1);
```



Assignment Rules ($:=$)

- **single assignment rule** – each variable may be assigned only once;

Illegal examples:

```
init(var) := ready;
```

```
init(var) := busy;
```

```
var := ready;
```

```
var := busy;
```

```
next(var) := ready;
```

```
var := busy;
```

```
next(var) := ready;
```

```
next(var) := busy;
```

```
init(var) := ready;
```

```
var := busy;
```

Assignment Rules ($:=$)

- **single assignment rule** – each variable may be assigned only once;

Illegal examples:

<code>init(var) := ready;</code>	<code>var := ready;</code>	<code>next(var) := ready;</code>
<code>init(var) := busy;</code>	<code>var := busy;</code>	<code>var := busy;</code>
<code>next(var) := ready;</code>	<code>init(var) := ready;</code>	
<code>next(var) := busy;</code>	<code>var := busy;</code>	

- **circular dependency rule** – a set of equations must not have “cycles” in its dependency graph, unless broken by delays (i.e. by `next()`); **Illegal** examples:

<code>next(x) := next(y);</code>	<code>x := (x + 1) mod 2;</code>	<code>next(x) := x & next(x);</code>
<code>next(y) := next(x);</code>		

Legal example:

<code>next(x) := next(y);</code>
<code>next(y) := y & x;</code>

DEFINE declarations

DEFINE <id> := <simple_expression>;

- similar to *C/C++ macro* definitions: each occurrence of the defined symbol is replaced with the body of the definition
- provide an alternative way of defining *output variables*;

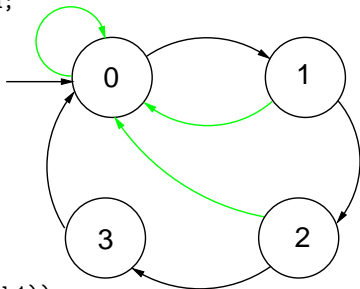
Example:

```
MODULE main
  VAR
    b0 : boolean;
    b1 : boolean;
  ASSIGN
    init(b0) := FALSE;
    next(b0) := !b0;
    init(b1) := FALSE;
    next(b1) := ((!b0 & b1) | (b0 & !b1));
  DEFINE
    out := toint(b0) + 2*toint(b1);
```

Example: modulo 4 counter with reset

The counter can be reset by an external “uncontrollable” signal.

```
MODULE main
VAR
  b0 : boolean; b1 : boolean; reset : boolean;
ASSIGN
  init(b0) := FALSE;
  init(b1) := FALSE;
  next(b0) := case
    reset = TRUE   : FALSE;
    reset = FALSE  : !b0;
  esac;
  next(b1) := case
    reset : FALSE;
    TRUE  : ((!b0 & b1) | (b0 & !b1));
  esac;
DEFINE
  out := toint(b0) + 2*toint(b1);
```



Exercise 1

Exercise:

simulate the system with `nuXmv` and draw the FSM.

```
MODULE main
VAR
  request : boolean;
  state   : { ready, busy };

ASSIGN
  init(state) := ready;
  next(state) :=
    case
      state = ready & request : busy;
      TRUE                    : { ready, busy };
    esac;
```

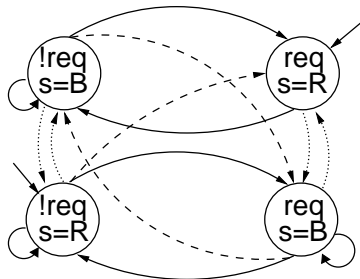
Exercise 1

Exercise:

simulate the system with `nuXmv` and draw the FSM.

```
MODULE main
VAR
  request : boolean;
  state   : { ready, busy };

ASSIGN
  init(state) := ready;
  next(state) :=
    case
      state = ready & request : busy;
      TRUE                     : { ready, busy };
    esac;
```



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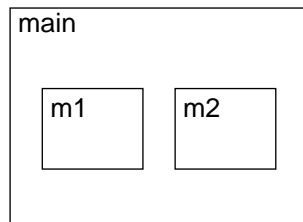
Modules [1/4]

An SMV program consists of one or more *module declarations*.

- each SMV program must contain a `main` module;
- modules can be **instantiated** in the VAR declaration of other modules;
- the variables declared within a module can be referred to via the dot notation (e.g., `m1.out`, `m2.out`).

Example:

```
MODULE counter
  VAR out: 0..9;
  ASSIGN next(out) :=
    (out + 1) mod 10;
MODULE main
  VAR m1 : counter; m2 : counter;
    sum: 0..18;
  ASSIGN sum := m1.out + m2.out;
```

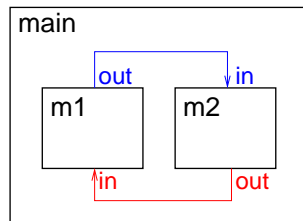


A module declaration can be *parametric*:

- a parameter is passed by reference;
- any expression can be used as parameter;

Example:

```
MODULE counter(in)
  VAR out: 0..9;
  ...
MODULE main
  VAR m1 : counter(m2.out);
      m2 : counter(m1.out);
  ...
```



Example: modulo 4 counter (revisited)

```
MODULE counter_cell(tick)
```

```
VAR
```

```
  value : 0..1;  
  done  : boolean;
```

```
ASSIGN
```

```
  init(value) := 0;  
  next(value) :=  
    case  
      tick = FALSE : value;  
      tick = TRUE  : (value + 1) mod 2;  
    esac;  
  done := tick & (((value + 1) mod 2) = 0);
```

```
MODULE main
```

```
VAR
```

```
  bit0 : counter_cell(TRUE);  
  bit1 : counter_cell(bit0.done);  
  out  : 0..3;
```

```
ASSIGN
```

```
  out := bit0.value + 2*bit1.value;
```

- Modules can be easily **composed**:

```
MODULE counter_4(tick)
VAR
  bit0 : counter_cell(tick);
  bit1 : counter_cell(bit0.done);
  out : 0..3; done : boolean;
ASSIGN out:= bit0.value + 2*bit1.value;
DEFINE done := bit1.done;

MODULE counter_64(tick) -- A counter modulo 64
VAR
  b0 : counter_4(tick);
  b1 : counter_4(b0.done);
  b2 : counter_4(b1.done);
  out : 0..63;
ASSIGN out := b0.out + 4*b1.out + 16*b2.out;
```

- a module without parameters and assignments can be seen as a simple **record**:

```
MODULE point
VAR
  x: -10..10;
  y: -10..10;
```

```
MODULE circle
VAR
  center: point;
  radius: 0..10;
```

```
MODULE main
VAR c: circle;
ASSIGN
  init(c.center.x) := 0;
  init(c.center.y) := 0;
  init(c.radius)   := 5;
```

Example: modulo 4 counter with reset (revisited)

```
MODULE counter_cell(tick, reset)
VAR
  value : 0..1;
ASSIGN
  init(value) := 0;
  next(value) :=
    case
      reset = TRUE : 0;
      TRUE : case
        tick = FALSE : value;
        tick = TRUE  : (value + 1) mod 2;
      esac;
    esac;
DEFINE
  done := tick & (((value + 1) mod 2) = 0);

MODULE counter_4(tick, reset)
VAR
  bit0 : counter_cell(tick, reset);
  bit1 : counter_cell(bit0.done, reset);
DEFINE
  out  := bit0.value + 2*bit1.value;
  done := bit1.done;
```

```
MODULE main
VAR
  reset : boolean;
  c : counter_4(TRUE, reset);
DEFINE
  out := c.out;
```

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Constraint Style Modeling [1/3]

```
MODULE main
VAR
request : boolean;  state : {ready,busy};
ASSIGN
  init(state) := ready;
  next(state) := case
    state = ready & request : busy;
    TRUE                     : {ready,busy};
  esac;
```

Every program can be alternatively defined in a *constraint style*:

```
MODULE main
VAR
  request : boolean;
  state   : {ready,busy};
INIT
  state = ready
TRANS
  (state = ready & request) -> next(state) = busy
```

Constraint Style Modeling [2/3]

- a model can be specified by zero or more constraints on:
 - *invariant states*:
INVAR <simple_expression>
 - *initial states*:
INIT <simple_expression>
 - *transitions*:
TRANS <next_expression>
- constraints can be mixed with assignments;
- any propositional formula is allowed as constraint;
- **risk of defining *inconsistent models!***
(i.e. INIT p & $!p$)
- not all **constraints** can be easily rewritten in terms of assignments!

TRANS

$$\text{next}(b0) + 2*\text{next}(b1) + 4*\text{next}(b2) = \\ (b0 + 2*b1 + 4*b2 + \text{tick}) \bmod 8$$

- Models written in **assignment style**:
 - by construction, there is always *at least one initial state*;
 - by construction, all states have *at least one next state*;
 - *non-determinism is apparent* (unassigned variables, set assignments...).
- Models written in **constraint style**:
 - INIT constraints *can be inconsistent*:
 - inconsistent model: no initial state
 - any specification (also SPEC 0) is vacuously true.
 - TRANS constraints *can be inconsistent*:
 - the transition relation is not total (there are deadlock states) (nuXmv can detect and report this case with the `check_fsm` command).
 - **Example**:

```
MODULE main
  VAR b : boolean;
  TRANS b -> FALSE;
```
 - *non-determinism is hidden*:

```
TRANS (state = ready & request) -> next(state) = busy
```

Example: modulo 4 counter with reset (constraint style)

```
MODULE counter_cell(tick, reset)
VAR
  value : 0..1;
  done  : boolean;
INIT
  value = 0;
TRANS
  reset = TRUE -> next(value) = 0
TRANS
  reset = FALSE -> ((!tick -> next(value) = value) &
                   (tick -> next(value) = (value+1) mod 2))
INVAR
  done = (tick & (((value + 1) mod 2) = 0));
...
```

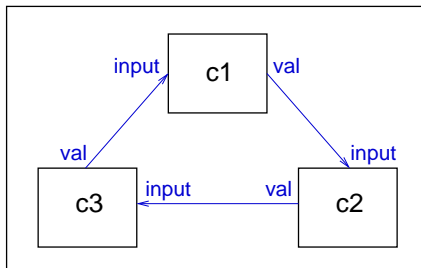
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Synchronous composition [1/2]

The composition of modules is **synchronous** by default:
all modules move at each step.

```
MODULE cell(input)
VAR
  val : {red, green, blue};
ASSIGN
  next(val) := input;

MODULE main
VAR
  c1 : cell(c3.val);
  c2 : cell(c1.val);
  c3 : cell(c2.val);
```



Synchronous composition [2/2]

A possible execution:

<i>step</i>	<i>c1.val</i>	<i>c2.val</i>	<i>c3.val</i>
0	red	green	blue
1	blue	red	green
2	green	blue	red
3	red	green	blue
4
5	red	green	blue

Asynchronous composition can be obtained using keyword `process`:
one process moves at each step.

```
MODULE cell(input)
VAR
  val : {red, green, blue};
ASSIGN next(val) := input;
FAIRNESS running

MODULE main
VAR
  c1 : process cell(c3.val);
  c2 : process cell(c1.val);
  c3 : process cell(c2.val);
```

Each process has a boolean `running` variable:

- true iff the process is selected for execution;
- can be used to guarantee a fair scheduling of processes.

Asynchronous composition [2/2]

A possible execution:

<i>step</i>	<i>running</i>	<i>c1.val</i>	<i>c2.val</i>	<i>c3.val</i>
0	-	red	green	blue
1	c2	red	red	blue
2	c1	blue	red	blue
3	c1	blue	red	blue
4	c2	blue	red	blue
5	c3	blue	red	red
6	c2	blue	blue	red
7	c3	blue	blue	blue

Warning: in `nuXmv` processes are deprecated!

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Mutual Exclusion [1/2]

```
MODULE user(semaphore)
VAR
  state : {idle, entering, critical, exiting};
ASSIGN
  init(state) := idle;
  next(state) :=
    case
      state = idle : {idle, entering};
      state = entering & !semaphore : critical;
      state = critical : {critical, exiting};
      state = exiting : idle;
      TRUE : state;
    esac;
  next(semaphore) :=
    case
      state = entering : TRUE;
      state = exiting : FALSE;
      TRUE : semaphore;
    esac;
FAIRNESS running;
```

Mutual Exclusion [2/2]

```
MODULE main
VAR
  semaphore : boolean;
  proc1 : process user(semaphore);
  proc2 : process user(semaphore);
ASSIGN
  init(semaphore) := FALSE;
```

Exercise:

- simulate a random execution of the “mutual exclusion” system;

Adder [1/3]

```
MODULE bit-adder(in1, in2, cin)
VAR
  sum : boolean;
  cout : boolean;
ASSIGN
  next(sum) := (in1 xor in2) xor cin;
  next(cout) := (in1 & in2) | ((in1 | in2) & cin);

MODULE adder(in1, in2)
VAR
  bit[0] : bit-adder(in1[0], in2[0], 0);
  bit[1] : bit-adder(in1[1], in2[1], bit[0].cout);
  bit[2] : bit-adder(in1[2], in2[2], bit[1].cout);
  bit[3] : bit-adder(in1[3], in2[3], bit[2].cout);
DEFINE
  sum[0] := bit[0].sum;
  sum[1] := bit[1].sum;
  sum[2] := bit[2].sum;
  sum[3] := bit[3].sum;
  overflow := bit[3].cout;
```

Adder [2/3]

```
MODULE main
VAR
  in1 : array 0..3 of boolean;
  in2 : array 0..3 of boolean;
  a : adder(in1, in2);
ASSIGN
  next(in1[0]) := in1[0]; next(in1[1]) := in1[1];
  next(in1[2]) := in1[2]; next(in1[3]) := in1[3];
  next(in2[0]) := in2[0]; next(in2[1]) := in2[1];
  next(in2[2]) := in2[2]; next(in2[3]) := in2[3];
DEFINE
  op1 := toint(in1[0]) + 2*toint(in1[1]) + 4*toint(in1[2]) +
    8*toint(in1[3]);
  op2 := toint(in2[0]) + 2*toint(in2[1]) + 4*toint(in2[2]) +
    8*toint(in2[3]);
  sum := toint(a.sum[0]) + 2*toint(a.sum[1]) + 4*toint(a.sum[2]) +
    8*toint(a.sum[3]) + 16*toint(a.overflow);
```

Exercise:

- simulate a random execution of the “adder” system;
- after how many steps the adder stores the computed final sum value?
- add a reset control which changes the values of the operands and restarts the computation of the sum

Example: model programs in nuXmv [1/4]

Consider the following piece of code computing the GCD:

```
void main() {  
  ... // initialization of a and b  
  while (a!=b) {  
    if (a>b)  
      a=a-b;  
    else  
      b=b-a;  
  }  
  ... // GCD=a=b  
}
```

Example: model programs in nuXmv [2/4]

Let's label the *entry point* and the *exit point* of every statement:

```
void main() {  
  ... // initialization of a and b  
11: while (a!=b) {  
  12: if (a>b)  
    13: a=a-b;  
    else  
    14: b=b-a;  
  }  
15: ... // GCD=a=b  
}
```

Example: model programs in nuXmv [3/4]

assignment style encoding:

```
MODULE main()
VAR  a: 0..100;  b: 0..100;
    pc: {11,12,13,14,15};
ASSIGN
  init(pc):=11;
  next(pc):=
    case
      pc=11 & a!=b: 12;
      pc=11 & a=b: 15;
      pc=12 & a>b: 13;
      pc=12 & a<=b: 14;
      pc=13 | pc=14: 11;
      pc=15: 15;
    esac;
```

```
next(a):=
  case
    pc=13 & a>b : a-b;
    TRUE: a;
  esac;
next(b):=
  case
    pc=14 & b > a: b-a;
    TRUE: b;
  esac;
```


Example: model programs in nuXmv [4/4]

constraint style encoding:

```
MODULE main
VAR
  a : 0..100;  b : 0..100;  pc : {11, 12, 13, 14, 15};
INIT pc = 11
TRANS
  pc = 11 -> (((a != b & next(pc) = 12) | (a = b & next(pc) = 15))
              & next(a) = a & next(b) = b)
TRANS
  pc = 12 -> (((a > b & next(pc) = 13) | (a < b & next(pc) = 14))
              & next(a) = a & next(b) = b)
TRANS
  pc = 13 -> (next(pc) = 11 & next(a) = (a - b) & next(b) = b)
TRANS
  pc = 14 -> (next(pc) = 11 & next(b) = (b - a) & next(a) = a)
TRANS
  pc = 15 -> (next(pc) = 15 & next(a) = a & next(b) = b)
```